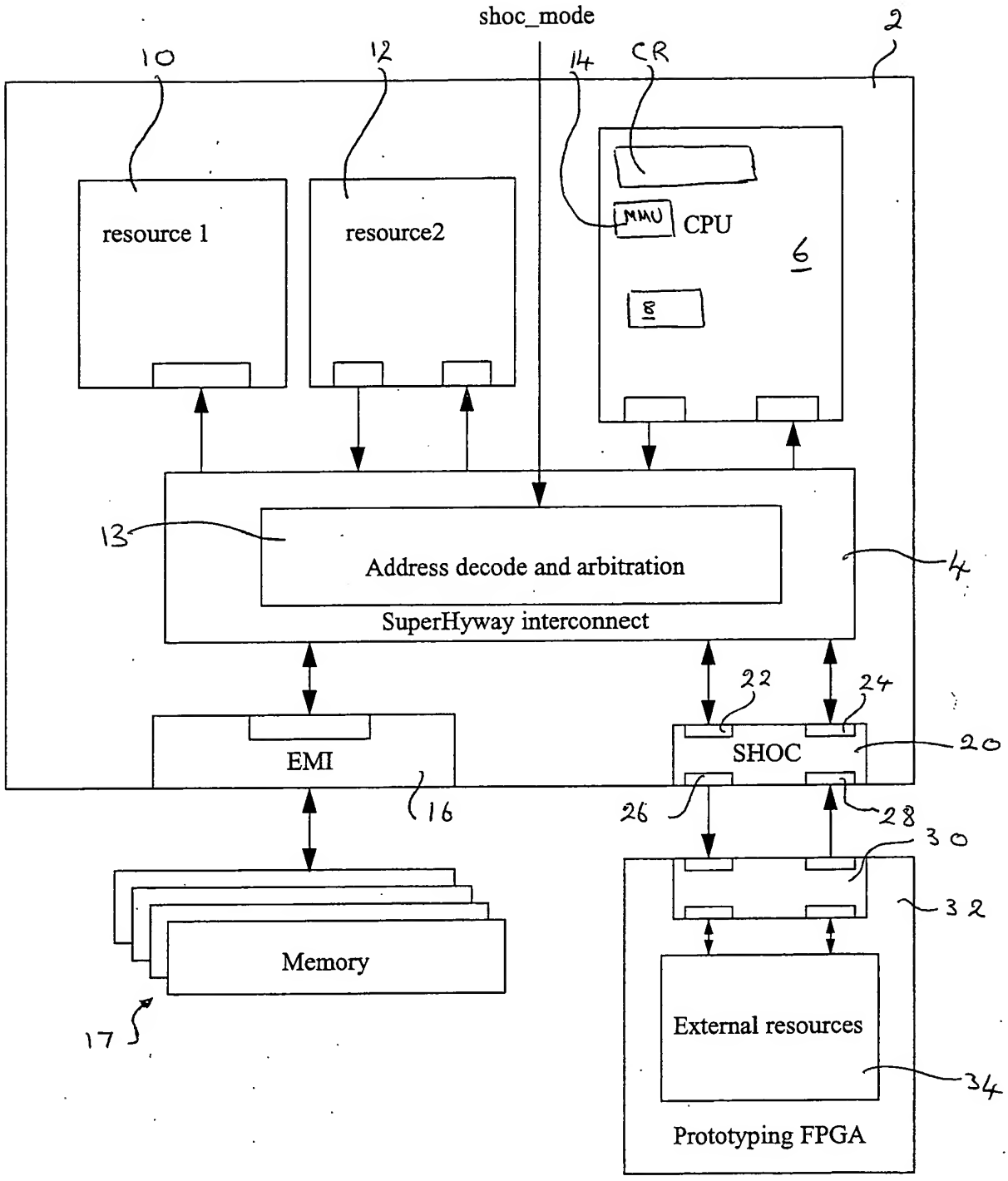


Figure 1

~~Integrated system~~

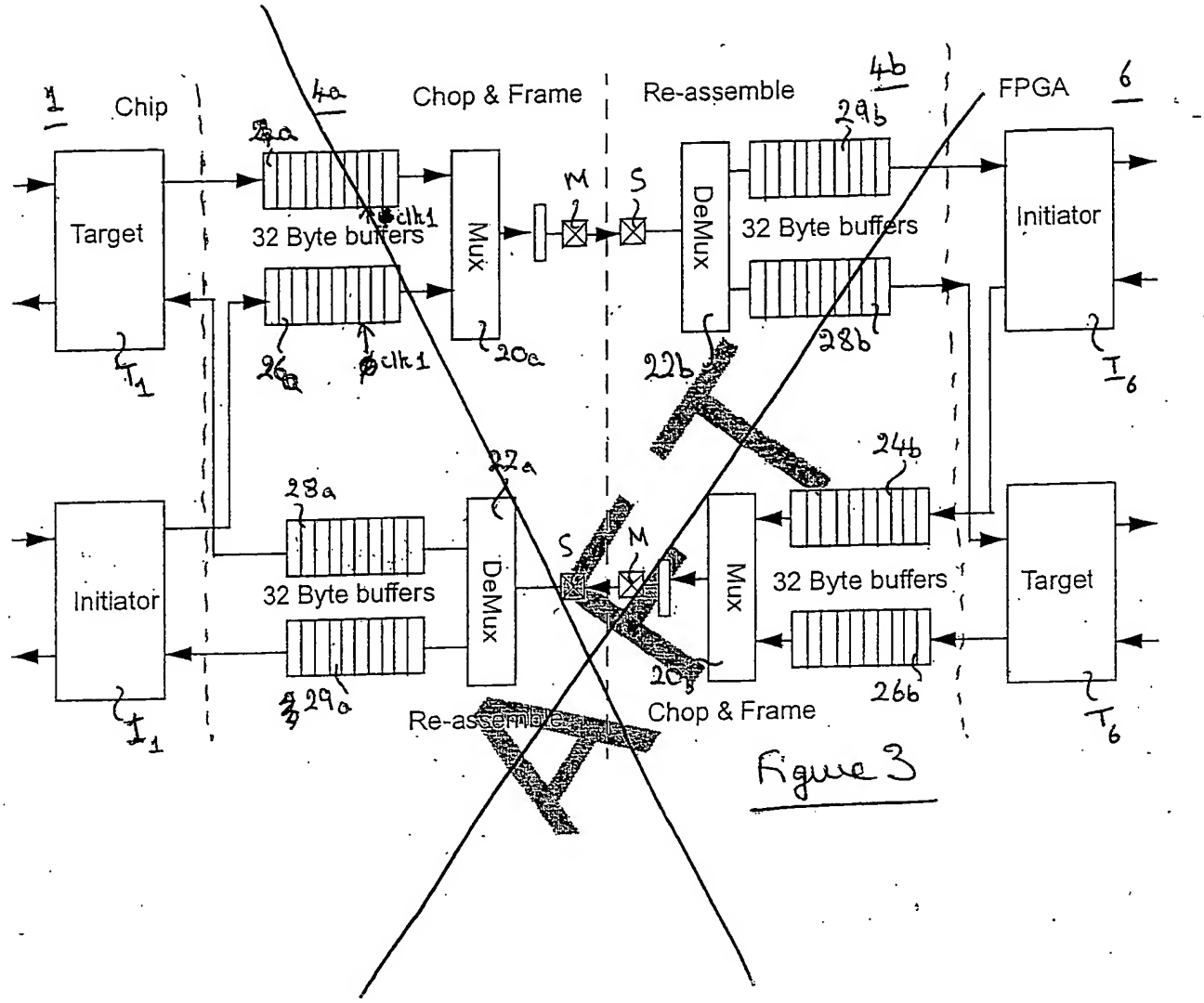


Figure 3

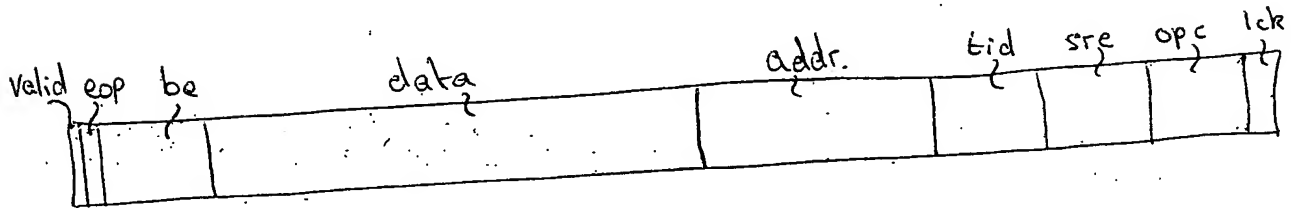
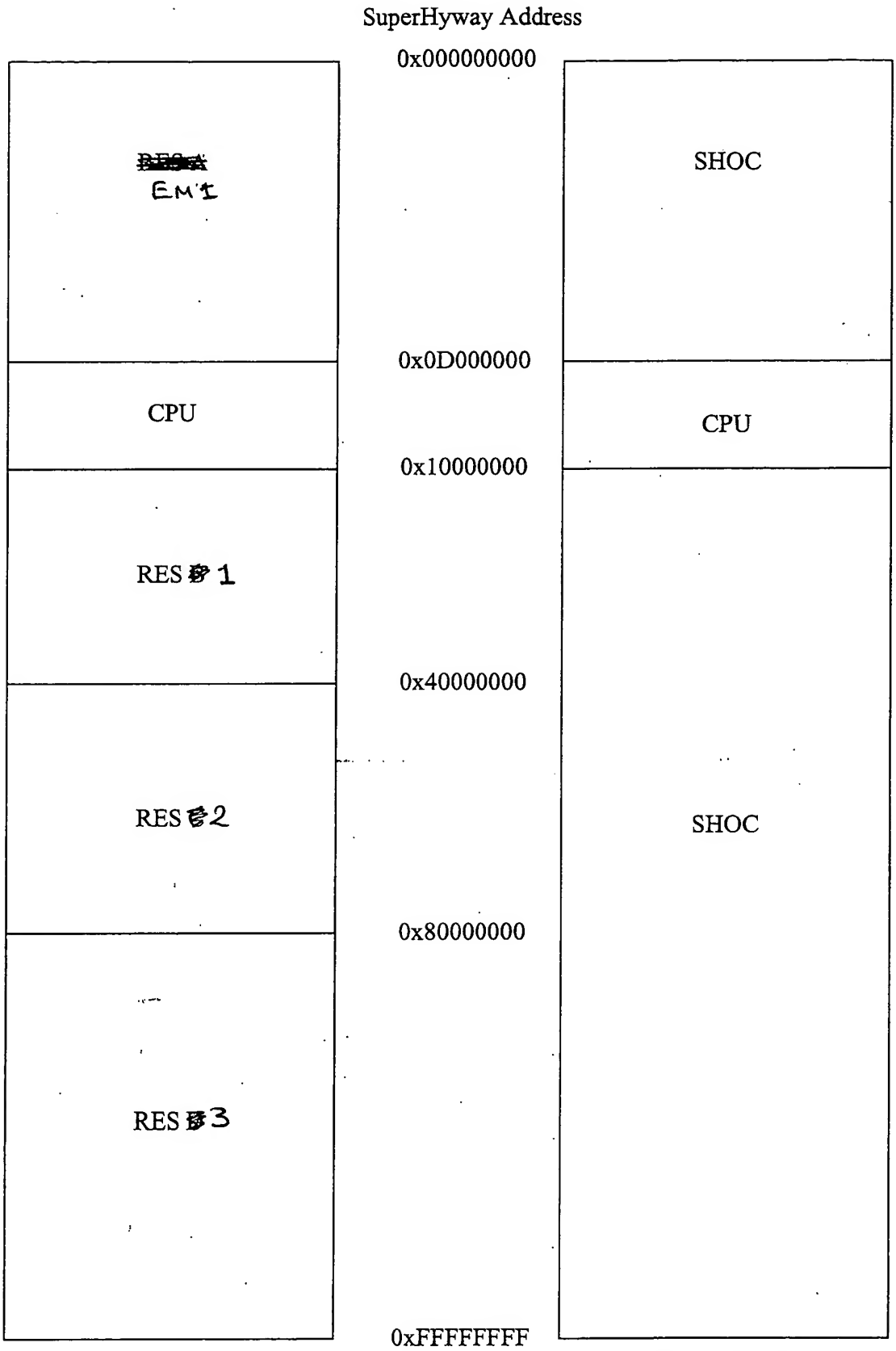


Figure 2



Dual Address maps

Figure 3

Figure 4

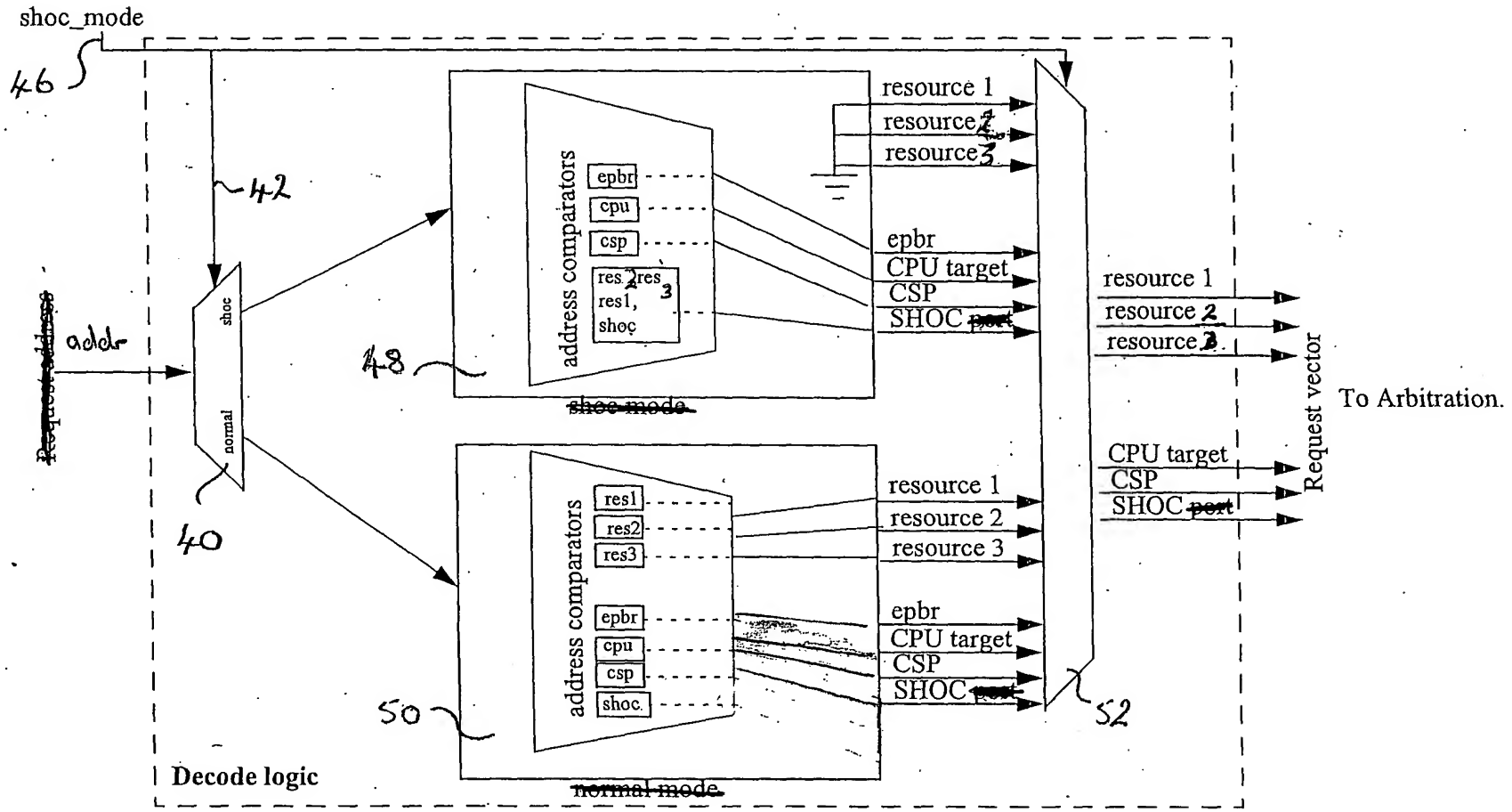

shoc_mode
46
42
addr
shoc
normal
40
48
address comparators
epbr
cpu
csp
res1, res2, res3
shoc
shoc mode
resource 1
resource 2
resource 3
epbr
CPU target
CSP
SHOC port
50
address comparators
res1
res2
res3
epbr
cpu
csp
shoc
normal mode
resource 1
resource 2
resource 3
epbr
CPU target
CSP
SHOC port
52
resource 1
resource 2
resource 3
CPU target
CSP
SHOC port
Request vector
To Arbitration.
Decode logic

Figure 5